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Production of beryllia hybrids for the CDF Run IIb silicon strip detector upgrade

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Abstract

A compact, lightweight beryllia hybrid has been designed for the CDF Run IIb silicon detector. The hybrid comes in two versions, a four-chip version for the outer layers (L1-L5) of the detector, and a two-chip version for the innermost layer (L0). After successful prototyping, the final version of the four-chip hybrid went into preproduction and 117 hybrids were produced. No significant technical problems were encountered during the project. The yield of good hybrids is $\sim 90\%$. This note describes the hybrid design features, production techniques, and the preproduction experience in detail.

1 Introduction

The CDF Run IIb silicon detector [1, 2] was designed to replace the inner layers (L00 and SVXII) of the current CDF silicon system. The new design provides tolerance for a radiation dose five times larger than the current detector, thus maintaining excellent tracking performance throughout Run IIb. The Run IIb design differs significantly from the current detector. In order to be radiation-hard, the silicon sensors are single-sided and must be cooled actively [3]. A new radiation-hard readout chip, the SVX4 chip, was designed and produced [4], and has been irradiated without any performance degradation for doses exceeding 20 MRad. A new compact module structure, the "stave", was developed for the outer layers (L1-L5) of the Run IIb detector [5,6]. Figure 1 shows an exploded view of the Run IIb silicon detector and illustrates the layer arrangement, stave and hybrid locations.

The stave hybrids sit directly on the silicon sensors. They are connected to the silicon strips via ceramic pitch adapters glued next to them. Power, control, data and high voltage connections to the hybrids are made from the stave bus cables through gaps between the sensors.

The design requirements of the hybrid and the overall system are closely intertwined. Because the single-sided sensors, the coolant, and the cooling structures contribute substantial material, the hybrid must be as compact and lightweight as possible to minimize further contributions. The hybrid must provide good electrical performance in deadtimeless operation despite being glued directly on top of the silicon sensors. The heat of the chips must flow efficiently through the sensors and the stave bus cable into the stave cooling pipes. Of course, the hybrid should also be robust and reliable. Finally, technological risks and significant R&D must be minimized to keep a tight schedule.

These requirements were satisfied by choosing a beryllia (BeO ceramic) hybrid type, which has been used in CDF before. (A polyimide hybrid might have been cheaper and lighter, but at the price of inferior thermal properties, possibly a less compact stave structure, a larger R&D effort and therefore more risk in terms of schedule and performance.)

This note documents the hybrid design criteria, layout, components, pre-production experience, yield, and performance.

2 Process

The hybrid substrate is beryllia (BeO). The substrate dimensions are 38 x 20 x 0.380 mm^3 for the the four-chip hybrid, and 22.5 x 33 x 0.380 mm^3 for the L0 hybrid. The substrate vendor is Brush Wellman Inc.[1]

The hybrid circuitry is produced by Circuits Processing Technology Inc. in a Dupont Fodel photo-printable thick film process [7]. By using photoimageable thick film materials, printing and pattern generation are separated and can be optimized independently. This leads to an increased resolution and density compared with "traditional" thick film technology. The Fodel

[1] A wholly-owned subsidiary of Brush Engineered Materials Inc.

process is reported to resolve 40 μm wide traces and 50 μm wide spaces over significant areas [8]. The minimum resolved via diameters are 75 μm for a 150 μm pitch.

For the CDF Run IIb hybrids, the minimum trace width is 125 μm and the minimum space width is 75 μm, with a minimum via size of 150 μm. These conservative choices were made to increase the expected hybrid yield and to reduce the hybrid costs.

Typical dielectric (Fodel 6050) thicknesses are 45 μm. The breakdown voltage over a thickness of 25 μm exceeds 1000 V. The gold conductor (Fodel 5771) is typically 8-12 μm thick. It is suitable for ultrasonic aluminum wedge and thermosonic gold ball bonding. A different, solderable PT/Pd/Ag conductor material is used for the top layer component pads (Fodel 4596).

3 Schematic and Layout

The schematic of the stave hybrid is shown in Figure 3. The stave hybrid carries four SVX4 chips. The hybrid receives and distributes analog and digital power to the chips, along with the control signals (8 single-ended CMOS control signals and 3 low-voltage differential signals (LVDS) [9]: back-end clock, front-end clock, and priority-in). The combined digitized data stream of the four chips is sent from the hybrid on an 8-bit LVDS bus. Three of the bus lines (bus 0, 1 and 3) are bi-directional and are also used to send control signals to the chip during digitization.

The hybrid is loaded with 30 passive surface-mount components. The complete part list is given in Table 1. Most resistors are used for control signal and data bus terminations. (The data bus termination is provided by a thin-film resistor array, which is placed and bonded on all hybrids. However, since only the last of a series of three hybrids on each side of a stave needs this termination, the bonds are pulled if no termination is needed.) There are two biasing resistors (for Islope to analog ground, and for IQUI to AVDD). One thermistor (RTD) serves as a temperature monitor.

Two ceramic decoupling capacitors (100 nF each), one for analog and one for digital power, are located near ($\sim$1 mm) each SVX4 chip in the small gap between adjacent chips. The location of the capacitors is visible on the picture in Figure 2 or the layout overview of Figure 4. There is one additional "big" ceramic decoupling capacitor of 4.7 μF for digital power. There was no room on the hybrid for a corresponding analog power decoupling capacitor. (Due to mechanical constraints of the height profile of a stave, the space in the upper right corner of the hybrid must not be covered by a tall component.)

The hybrid also carries a simple RC low-pass high voltage filter. The corresponding capacitor is again relatively tall (1.25 mm), not because of its capacitance but in order to achieve a high breakthrough voltage. (The filtered high voltage line is bonded to the stave bus cable, which in turn is connected to the sensor back plane with electrically conducting silver epoxy.)

Crucial for the electrical performance of the hybrid are its ground connections. On the hybrid, analog, digital and high voltage ground are all connected together. The SVX4 chip is a mixed-signal ASIC designed for deadtimeless operation [10]. The low resistivity substrate of its bulk CMOS process is exploited to carry all analog ground currents and effectively decouple

the low noise analog section from the ("noisy") digital section of the chip. This implies that the front-end section of the chip sits on a conducting (ground) pad, and that analog and digital ground are connected on the hybrid. The connection is realized by multiple bonds on the hybrid. The high voltage ground to hybrid ground connection is permanent.

The hybrid material is responsible for 13% of the total radiation length of the stave,[2] which is significantly better than achieved for the Run IIa detector. The improvement is due to the high circuit densities that can be realized with the Fodel process, producing hybrids of smaller area and fewer layers. A detailed hybrid material balance is compiled in Table 4.

Of the total contribution of the hybrid, the hybrid substrate, despite being BeO, adds much material (24% of the hybrid total) simply because it is much taller (380 μm) than the print layers. The four conductor layers are thin but correspond to $\sim$ 30% together because gold is a high-Z material. The seven dielectric layers add 24%. (In order to protect the hybrid from bending due to changes in temperature, there are always two dielectric layers between every pair of conducting layers.) The remaining fraction is due to the passive components and the SVX4 chips. For a full list of layers, see Table 3.

The overall packing efficiency (the percentage of the hybrid area covered by chips) is 30.7%.

The bottom conductor layer covers the full area of the substrate and serves as an electric shield between the silicon strips and the upper hybrid circuitry. This layer is connected with a wide via ($\sim$500x500 μm^2) to the analog ground in layer 7. The other conductor layers are shown in Figures 5 to 8. The power and ground layers (Figures 5 and 6) have a similar structure. A wide gold strip covers the upper part of the hybrid and extends from the top to roughly the end of the front-end section of the chips (preamplifier and pipeline). This strip is connected to the analog power and analog ground pads, respectively. Below, a corresponding strip under the back-end section of the chip provides digital power and ground, respectively. The remaining space is used for various traces. The top gold layer (Figure 7) contains the bond pads for bonding the chips to the hybrid and the hybrid to the stave bus cable, various traces, and four wide gold pads to which the SVX4 chips are glued with conducting silver epoxy. The large pad at the corner of the hybrid next to the LBNL logo provides the ground connection to the stave bus cable aluminum shield.

A bonding diagram is given in Figure 9. The hybrid-to-stave bond pads are divided in three sections by two strips of dielectric coverlay. This minimizes the possible peeling off of the gold trace when pulling the wire bonds to the test PCB before module construction and makes rework during stave construction easier.

4 Hybrid production and assembly

After the delivery of the hybrid substrates to LBNL, the hybrids are assembled and bonded at various Silicon Valley firms with testing and encapsulation taking place at LBNL. Each major

[2] Overall, the stave corresponds to $\sim$ 1.4% X_0. This number considers the silicon detectors, coolant, bus cable, carbon fiber, foam, glue, hybrids, mini-port card, etc.

production step is organized and monitored closely by a single institution, LBNL. This arrangement ensures fast feedback on production quality, best communication, and a minimum of shipping.

A user-friendly and robust web-based database was set up by UC Davis and was used extensively to document significant production steps and organize the hybrid test data.[3]

The major production steps are described in detail below.

4.1 SVX4 chip delivery

The SVX4 chips are produced by TSMC [4] on 200 mm (8-inch) wafers in a commercial, five metal layer, 0.25 μm CMOS process. The wafers are background from their original thickness (700 μm) to 300 μm which reduces material and thus their contribution to the radiation length. The background wafers are polished, and backplated with a thin gold film (0.25 μm Au on 0.5 μm Cr). This ensures good electrical contact from the top of the chip through the low-resistivity substrate to the hybrid ground pad where the chip is glued. The backgrinding and polishing is performed by Aptek Industries,[5] and the plating is done by Scientific Coating Labs.[6]

The background and backplated wafers were probed at FNAL. A large set of chip characteristics were tested, including power consumption, proper initialization, pedestal/gain homogeneity, noise and much more. Much of the wafer probing hardware and software was developed by LBNL and was also used for hybrid testing, allowing for a direct comparison of wafer and hybrid measurements for a given die which helped to perform detailed system cross-checks. Wafer and hybrid data were found to match well. Details on the correlation of wafer and hybrid measurements and their yields are given in section 5.

After wafer probing the wafers were sent to dicing at American Dicing.[7]

4.2 Substrate testing

The bare hybrid substrates were delivered to LBNL in three batches of 46, 116 and 18 substrates. All hybrids were visually inspected and then manually checked for power shorts and opens with probe needles. The power short and open check looked at the resistance for each pair of the large AGND, AVDD, DGND, and DVDD bond pads at the bottom of the hybrid to make sure it was as expected (open for all pairs, except for AGND-DGND which should be close to zero).

One hybrid per batch was inspected in more detail by manually checking all traces for opens/shorts using two microprobes. This procedure takes a couple of hours. It was not practical and not necessary to have a detailed inspection for more than one hybrid substrate per batch.

Four of 130 bare hybrids failed the power short tests, and another one was damaged on the pads during probing.

[3] The database is located at http://cdfw09.ucdavis.edu; to view data, log in using “guest”/”guest”.

[4] Taiwan Semiconductor Manufacturing Company

[5] 414-F Umbarger Road, San Jose, CA 95111, (800) 363-4363, http://www.aptekindustries.com.

[6] 350 Martin Ave., Santa Clara, CA 95050, (800) 893-3669, http://www.wso.net/scl/.

[7] 344 East Brighton Ave., Syracuse, NY 13210, (315) 428-1200, http://www.americandicing.com.

4.3 Assembly of passive components and die attach

Hybrid assembly (the loading of passive components and the die attachment) was done by Advanced Assemblies, Inc.[8]

LBNL received the diced wafers from Fermilab, removed the bad chips and the SVX4.2A chips[9], and sent the good and fair chips to the company. A chip was considered good if it had no bad pipeline capacitors or other defects; fair if it had exactly one bad pipeline capacitor; and bad if it had more than one bad pipeline capacitor, a bad channel, or other defects. Bad chips were rejected. We did not presort the chips in the waffle packs, so the fair chips were randomly distributed throughout the hybrids. Three hybrids with three fair chips were produced, and no hybrid had four fair chips. Ideally, one would use only good chips or avoid using several fair chips on a single hybrid.

The hybrid substrates were labeled with a fine pen (serial numbers h1-h130). This enabled the assembly company to keep track of the chips and enabled the comparison of wafer probing and hybrid data for a given die.

The assembly company received the hybrids in several batches of forty hybrids and an initial batch of ten, in order to start the process. The cost was $\sim$ \$70/piece for a batch of 80 hybrids and a lead time of two weeks. In practice the company would likely need less than a day for loading the surface-mount passive components using a modern medium-size pick and place machine and a multi-zone reflow oven. The SVX4 chips and the termination chip resistor array are attached manually, which would likely take another full day.

The passive components are soldered with a water soluble solder paste.[10] The SVX4 chips are attached with a conducting silver epoxy [11] in order to allow the easy exchanging of bad chips.[12] The resistor chip is glued with a non-conductive five-minute epoxy.

After assembly and die attach, a quality assessment was performed by LBNL at the assembly company. The hybrids were carefully inspected visually. No further resistance measurements were performed. The hybrids were then put into the hybrid holder aluminum boxes by LBNL personnel. (The aluminum hybrid box consists of a aluminum lid and a machined aluminum base plate. The base plate is big enough to carry the hybrid and the test PCB with the Samtec connector.) The aluminum boxes were labeled and their lids closed (by screwing them onto the baseplate).

Inspecting the hybrids at the company rather than at LBNL saved 2-3 days of shipping time and minimized handling (opening and closing of the hybrid lids). The hybrids were then directly shipped by LBNL to the bonding company.

[8] 3014 Lawrence Expressway, Santa Clara CA 95051, (408) 992-0163.

[9] A reticle contained five SVX4.2B chips and one SVX4.1A chip. The A chips have the same functionality as the B chips, but differ in details of the front-end decoupling and the ADC comparator circuitry.

[10] WS 483 from AIM. See http://www.aimsolder.com

[11] BiPax, TRA-DUCT 2902, TRA-CON Inc.

[12] Removal of bad chips proceeds in several steps. First, the hybrid aluminum base plate is preheated. Then, the top of the bad chip is briefly heated with a wide area solder iron tip and removed. The procedure is straightforward, quick and reliable. Spill of molten epoxy on neighbouring pads, bond pad contamination, or rebonding turned out not to be a problem.

4.4 Bonding of hybrids

The bonding diagram of the hybrid is shown in Figure 9. There are 198 bonds from the SVX4 chips to the hybrid, 18 bonds from the resistor chip to the hybrid, 3x2 bonds between the AGND and DGND pads on the hybrid, and $\sim$ 74 bonds from the hybrids to the test PCB.

The quality of the wire bonding is crucial for the reliability of the hybrid and the amount of rework necessary. In order to not depend on a single vendor we explored two different Silicon Valley companies and also set up an older automatic bonder at LBNL as a fallback solution. Bonding at one of the companies was without problems, and the other company was less good, though acceptable, and most of the wire bonding was eventually done by industry. Typical bonding costs were $35 per hybrid.

All interconnections mentioned above, including those to the PCB, are done with thermosonic gold ball bonding. The gold wire thickness is 25 μm. This technique proved to be reliable and to be beneficial for occasional rework (chip replacement or rebonding). The heating of the hybrids and aluminum base plates did not pose a problem or inconvenience. Before bonding the hybrid was plasma cleaned which improved the bond strength significantly. The bond pull strength was tested routinely. The average pull strength measured in these tests was $\sim$ 10 grams and varied between 7 and 14 grams. The pull strength of the interconnections from the hybrid to the PCB, which are removed before module construction, was not tested.

4.5 Inspection and electrical tests of bonded hybrids

After bonding, the hybrids were inspected in detail at LBNL. Thorough testing of hybrids ensures high quality silicon modules. The testing must be done quickly in order to give fast feedback to the assembly and bonding companies. Since the hybrids are much more expensive than the chips (ignoring the SVX4 design cost), high yield is crucial. The testing and quality control procedures help to ensure an overall high yield.

The tests were as follows:

1. The hybrid was visually inspected to make sure that everything looked in order (no obviously broken, touching, or missing bonds, all components properly mounted, no dust, etc.) This was a quick check taking only a few minutes.

2. The hybrid was checked to make sure that there were no power shorts or opens. If power shorts occurred at this stage, it was usually because a chip had been damaged in the bonding process and developed an internal short rather than anything wrong with the substrate (which had already been checked). This was also a quick check.

3. Next, the hybrid was checked with the Svxscope test program[13] to make sure that basic DAQ was functioning. This was to make sure that the hybrid looked operational and that there were no obvious errors in the performance. One of our test stations (a PC with the

[13]The Svxscope program is a simple DAQ test program for the PC which provides graphical, realtime display of data from SVX4 chips or hybrids.

PATT3 and SVX4 scrambler printed circuit boards [11]) was dedicated to this check. This also was a quick check.

In general, if a hybrid passed these first three tests, then it was very likely to pass htwish. Only three hybrids had problems which did not show up somewhere during this initial check.

4. Finally, a full analysis using the htwish hybrid analysis program [12] was performed. This performs a full suite of tests checking all aspects of hybrid performance. This takes approximately 15 minutes to complete, and two of our test stations were dedicated to this testing, typically with both running in parallel.

In total, four test stations were used. One was used for quick hybrid tests with Svxscope. This station was also equipped with a manual probe station and an oscilloscope to help debug less obvious hybrid problems. Since the hybrid yield was high, time-consuming failure searches were rare. Two more test stations were fully dedicated to running automated hybrid tests with htwish. A fourth station was set up to run the PTS DAQ [13], but was mainly used to enter data into the hybrid data base rather than for testing.

A set of 20 hybrids could be processed in one day by two people. The nominal rate of 40 hybrids/week is not limited by testing. Two to three times the nominal rate would be achievable if necessary.

4.6 Encapsulation

Encapsulation of the hybrid bond connections was judged essential after the breaking of wire bonds in the Run IIa hybrids was observed. (The Lorentz forces due to current oscillations in the bond wires can cause resonant mechanical vibrations and subsequent bond breaking. The effect depends on the orientation of the bonds in the magnetic field of the CDF detector and the detector readout frequency/trigger rate, which may come close to the bond wire resonance frequency [14].)

As encapsulant we use Sylgard 186 from Dow Corning, a transparent silicone elastomer which cures at room temperature.

All but a few bonds are encapsulated at LBNL. The bond connections to the PCB are not encapsulated since they serve for testing purposes only and are removed before module assembly. Also the row of the bus termination resistor bonds near the PCB are not encapsulated. These bonds are close to the bonds to the PCB, and it is difficult to avoid the encapsulant spreading into the PCB bonds (see Figure 10). Also, 2/3 of the hybrids don't need the termination and so these bonds have to be pulled anyway. For the 1/3 of the hybrids which need to be terminated, the encapsulation can conveniently be combined with that of the bonds to the stave bus cable.

Encapsulation requires a good deal of practice and experience, and was very time-consuming, but it was not difficult for an experienced technician. Typically one person could encapsulate $\sim$ 10 hybrids per day. The most delicate wire bonds are the group of three near the input pads of the chips (see Figure 11). For these using a 0.4 mm diameter syringe (AWG 26) proved helpful. The other bonds can best be encapsulated with a 0.5 mm diameter syringe (AWG 24) which

makes the process faster. Directly after encapsulation, the hybrids are cured at 100°C, which helped prevent the encapsulant spreading out into the input pad region.

Encapsulation was the bottleneck of hybrid production at LBNL. With the preproduction procedures a hybrid production rate well above 40 hybrids/week could be obtained. If the rate was to be doubled or so, we would have to arrange encapsulation differently.

In a few cases, we had cured encapsulant spill onto the input bond pads (when a new technician was learning how to encapsulate hybrids). In most of these cases, we were able to remove the encapsulant from the bond pads without any major difficulties. A few of the hybrids sustained some damage to the bond pads when we attempted to remove the encapsulant. Those for which the encapsulant was successfully removed displayed no further problems. We anticipate that this would not be a problem in production, since the technicians would rapidly become familiar with the encapsulation procedure.

After the encapsulation a visual inspection of the hybrid and quick electrical functionality test is made (using the Svxscope program) to make sure that the hybrid performance has not been changed by encapsulation. This takes $\sim$ 5 minutes per hybrid. Much of this time is spent opening the hybrid box lids, connecting to the power supply, filling in the travelers, etc.

4.7 Burn-in at UC Davis

All hybrids are burnt in for typically 72 hours at UC Davis. During burn-in the hybrids are powered, clocked and run continuously with a standard pattern. Every 10 minutes the read-out consistency of the data is checked automatically. At the beginning and the end of the burn-in time a full htwish/htest test sequence is performed, which the hybrid must pass.

The failure rate during burn-in is small. More than 100 hybrids entered the burn-in procedure, but not a single hybrid failed it.

The burn-in hardware consists of a multi-port version of the LBNL scrambler boards (multi-scrambler board). Currently, there are four boards with eight hybrid spots each. Thus 64 hybrids can be burnt in in a 6-day week, which is well above the nominal 40 hybrids/week.[14]

The burn-in procedure, hardware, software and results are described in detail in a separate CDF note [15].

4.8 Final functionality check at FNAL

The hybrids are sent from Davis to FNAL. At FNAL they are run through a series of basic electric performance test on the PTS DAQ system before they are placed on a module. The htwish software package has been adopted to run on the PTS, but is not currently used.

[14] It would be straightforward to achieve an even larger rate.

5 Hybrid yield and performance

The following statistics break down the total yield of standard hybrids through the various stages of preproduction.

- **180** standard hybrid substrates were delivered.
  - 5 substrates were rejected for defects.
  - 10 substrates were used for the first batch of "pre-preproduction" hybrids and to get test samples from the assembly and bonding companies. These hybrids differ somewhat from the rest and are not considered below. Four of these hybrids were used for various high dose irradiation tests.
  - 46 substrates were not used.
- **119** substrates were sent to stuffing and bonding.
  - 1 hybrid was broken during stuffing and bonding.
  - 1 hybrid was not bonded.
- **117** standard hybrids were produced.
- **108** hybrids passed initial testing (including 5 which were repaired).
  - 2 hybrids failed due to having more than one bad capacitor on a chip.
  - 1 hybrid was broken during repair.
  - 1 hybrid had a malfunctioning RTD (this is easy to repair, and will be repaired).
  - 5 hybrids had some signals not functioning properly.
- **101** hybrids were successfully burned in.
  - 5 hybrids were damaged during encapsulation after passing initial testing.
  - 2 hybrids were kept by LBL after initial testing in case further tests were needed.

Overall, 104 out of the 117 produced hybrids were usable, for a total yield of 89%.

6 Chip yield

The hybrid yield depends crucially on the chip yield and the quality of the wafer probing.

A total of 895 SVX4.2B chips were delivered. (The SVX4.2A chips which are contained in the same waffle packs are not considered below since they were not used for preproduction. Generally these chips were perfectly functional and should have the same yield as the SVX4.2B chips.) Of these 895 chips, 81 had incomplete testing data: chips which were not tested, chips for which the tests did not complete due to poor contact of the wafer probing needles with the

wafer, or chips which were incorrectly tested. An additional 32 had inconclusive testing data: these chips were probably good, but failed due to high noise. In our experience, this noise was an artifact of the wafer probing process rather than a defect with the chip, and we successfully used a large number of similar chips in our hybrids without any problems. However, we could not safely conclude that they were good without actually using them.

The remaining 782 chips break down as follows:

Good chips: 500 (63.9%) (no bad pipeline capacitor or other problems)

Fair chips: 117 (14.9%) (exactly 1 bad capacitor)

Bad chips: 165 (21.1%):

- 81 were bad chips because they had more than 1 bad capacitor (but were perfect otherwise):
  - 46 had exactly **2 bad capacitors**.
  - 19 had exactly **3 bad capacitors**.
  - 8 had exactly **4 bad capacitors**.
  - 8 had **5 or more bad capacitors**.
- 59 were bad chips because they had **1 bad channel**.
- 25 were bad chips that had **other problems**.

The overall chip yield for good and fair chips is thus 79%.

It should be noted that each chip has 128x46=5888 pipeline capacitors. If one of these fails it is a minor effect and much less important than a bad channel. Less stringent selection criteria have been used for other projects and would lead to a even larger yield.

The agreement between the chip data obtained from wafer probing and the chip data as they performed upon being used in hybrids is excellent. Of the 460 chips which were tested after being installed into hybrids, there were a total of seven bad capacitors which appeared in hybrid testing which had not been detected in wafer probing. Four of these were due to capacitors which had just barely passed the cuts in wafer probing but were slightly worse in hybrid testing. The other three were masked by high noise during wafer probing, but better handling of the high noise problems during wafer probing would have allowed them to be detected.

7 L0 hybrid

The inner layer (L0) of the Run IIb detector requires only 72 hybrids. The L0 R&D was less time-critical than the stave design and was less advanced. L0 hybrid preproduction was a lesser priority and not on the critical path. It was partly done with prototype components, and only 16 preproduction L0 hybrids were produced.

The L0 hybrids differ from the stave hybrids in several respects. First, the sensors of the innermost silicon layer are only about half as wide as the outer (stave) layers, and the L0 hybrids carry only two SVX4 chips. Second, the chip input pads are not bonded to a pitch adapter which is directly connected to the sensors, but to a fine pitch cable that is glued on the top of the hybrid and extends $\sim$60 cm to the sensors. Space is very limited at small radii, and this configuration allows us to place the L0 hybrids outside the active detector volume at larger z coordinate values. Unlike the four-chip hybrid, the L0 hybrid receives differential (LVDS) signals for the eight normally single-ended control signals (CHMODE, BEMODE, FEMODE, L1A, PARST, CALSR, PRD1, and PRD2). A transceiver chip on the hybrid converts these signals to the single-ended CMOS standard the SVX4 chips require. The transceiver chip is a custom radiation-hard 0.25 μm CMOS ASIC designed by FNAL [16]. It is produced by TSMC using the same process as for the SVX4 chips.

Finally, the sensor high voltage, power, data bus, and control signals are not provided by wirebonds from a stave bus cable. Instead two flexible copper/polyimide/aluminum cables, with one running on top of the other, are soldered on the bottom of the hybrid.

Apart from these differences the L0 hybrid layout is similar to the stave hybrid. The production techniques are identical and the same companies produced the two hybrids.

Figures 12 to 17 show the schematics and the conductor layer Gerber files of the L0 hybrid. The bonding scheme is shown in Figure 18.

Because of the lower priority of the L0 hybrids, some small compromises were made in the L0 hybrid design and production. Only one version of the L0 hybrids was produced which performed well. In order to provide a first set of L0 hybrids early, a preliminary set of the HV, power, bus and control signal cables was produced before the final cables' pinout and connector sizes were specified. For simplicity the cables are much wider than necessary, the aluminum shield layer connections are probably not optimum, and the cheapest vendor was selected. Due to the cancelation of the project, the final L0 cables were never designed or produced.

Fifty L0 substrates were available for prototyping and preproduction. In preproduction 16 L0 hybrids were produced; nine of them performed fine, and one showed instabilities during burn-in which have not been investigated yet. Bonding of the L0 hybrids was done at LBNL.

There were no significant technological difficulties. In particular, the soldering of the cables to the hybrids worked very well. The preproduction batch of the L0 hybrids, however, was produced with the leftover cables from prototyping (since the final L0 cables were never produced), and the lower quality cables necessitated a number of repairs to correct opens in the cables. The cables also were responsible for 5 of the failed L0 hybrids.

8 Summary

During preproduction 117 stave hybrids and 16 L0 hybrids were produced. The yield of the stave hybrids was close to 90%. Hybrid preproduction ran fairly smoothly, and no significant technological difficulties were encountered. The quality of the selected SVX4 chips was excellent, and the correlation of wafer probing data and hybrid measurements of the same chips was

very good. There are no indications that the 90% yield could not be kept or exceeded in the full production of $\sim$ 1500 hybrids needed for the (now cancelled) Run IIb mass production.

During preproduction the hybrids were not continously produced at a fixed rate but in several batches, typically 40 hybrids each. The preproduction experience shows, however, that the nominal rate of 40 hybrids per week can easily be achieved in regular mass production. Only very few modifications (for example, in the encapsulation set-up) would be needed to increase the rate substantially, and doubling the production rate would be quite possible.

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[14] G. Bolla *et al*, "Wire bonds failures induced by resonant vibrations in the CDF silicon detector", http://www-cdf.fnal.gov/upgrades/silicon/ TASK-Force/N44-2-v3.pdf.

[15] A. Soha *et al*, "Burn-In of Hybrids for the CDF RunIIb Silicon Detector", CDF Note CDF/DOC/TRACKING/PUBLIC/6898.

[16] G. Cardoso, J. Hoff, A. Shenai and S. Zimmermann, "Ten Bits Differential Transceiver (0.25 μm)", FNAL Note, Document #ESE-SVX-020502 (July 26, 2002).

[17] G. Cardoso *et al.*, "Polyimide and BeO Mini Portcard Performance", submitted to IEEE Trans. Nucl. Sci., 2003.

Part	Value	Rating	Supplier	Part number	#	Size	Purpose
			Resistors				
R1-R4	36 kΩ	5%	Garrett	MCR01JW363E	4	0402	biasing resistors for Islope (to AGND)
R5-R8	7.7 kΩ	5%	Garrett	MCR01JW702E	4	0402	biasing resistors for IQUI (to AVDD)
R9-R11	75 Ω	5%	Garrett	MCR01JW750E	3	0603	termination resistors for FEClk, BEClk, PRIN
R12	1 kΩ	5%	Garrett	MCR01JW102E	1	0603	HV low-pass filter
R13	1 kΩ	5%	Garrett	MCR01JW102E	1	0603	VCAL low-pass filter
R14	RTD	5%	Semitec	103KT1608-1P	1	0603	temperature sensor
R25-R32	75 Ω	2%	MSI	MSRA8-SN-75R000G-G	1	8-array	termination resistor chip for bus0 - bus7
			Capacitors				
C1-C4	100 nF	10% 16V	Panasonic	ECJ1VD1C104K	4	0603	analog decoupling caps (near chip)
C6-C9	10 nF	10% 16V	Panasonic	ECJ0EB1C103K	4	0402	decoupling caps (ISET - AVDD)
C10-C13	100 nF	10% 16V	Panasonic	ECJ1VD1C104K	4	0603	digital decoupling caps (near chip)
C14	100 nF	10% 16V	Panasonic	ECJ1VD1C104K	1	0603	VCAL low-pass filter (VCAL-AGND)
C15	10 nF	10% 630V	Murata	GHM1530-B-103-K-630	1	1206	HV low-pass filter (HVout-AGND)
C16	4.7 μF	20% 16V	Panasonic	ECJ3YF1C475Z	1	1206	big/far digital decoupling cap
			ICs				
U1-U4	SVX4	—	LBNL/FNAL	—	4	—	

Table 1: Component list (four-chip hybrid)

Part	Value	Rating	Supplier	Part number	#	Size	Purpose
			Resistors				
R1-R2	36 kΩ	5%	Garrett	MCR01JW363E	2	0402	biasing resistors for Islope (to AGND)
R3-R4	7.7 kΩ	5%	Garrett	MCR01JW702E	2	0402	biasing resistors for IQUI (to AVDD)
R5-R6, R8	100 Ω	5%	KOA	RK73B1JLTD102J	3	0603	termination resistors for FEClk, BEClk, and PRIN
R7	1 kΩ	5%	KOA	RM73B1ET102J	1	0603	VCAL low-pass filter
R9	1 kΩ	5%	KOA	RM73B1ET102J	1	0603	HV low-pass filter
RN1	100 Ω	5%	Rohm	MNR18EOAPJ101	1	1608x8	termination chip for signals for transceiver chip
			Capacitors				
C1-C2	100 nF	10% 16V	Panasonic	ECJ1VB1C104K	2	0603	analog decoupling caps (near chip)
C3-C4	10 nF	10% 16V	Panasonic	ECUE1C103KBQ	2	0402	ISET decoupling caps (to AVDD)
C5-C6	10 nF	10% 16V	Panasonic	ECUE1C103KBQ	2	0402	ISET decoupling caps (to AGND)
C7-C8	100 nF	10% 16V	Panasonic	ECJ1VB1C104K	2	0603	digital decoupling caps (near chip)
C9	10 nF	10% 630V	Murata	GHM1530-B-103-K-630	1	1206	HV low-pass filter (HVout-AGND)
C10	100 nF	10% 16V	Panasonic	ECJ1VD1C104K	1	0603	VCAL low-pass filter (VCAL-AGND)
C11	4.7 μF	20% 16V	Panasonic	ECJ3YF1C475Z	1	1206	large hybrid digital decoupling cap
			ICs				
U1-U2	SVX4	—	LBNL/FNAL	—	2	—	
U3	XCVR	—	FNAL	—	1	—	transceiver chip

Table 2: Component list (L0 hybrid)

Layer	Type	Description	Material
1	conductor	shield layer	Fodel 5771 (gold)
2	dielectric	first dielectric layer	Fodel 6050 (dielectric)
3	via fill	first via fill layer	Fodel 5727 (gold)
4	conductor	power and 1st trace layer	Fodel 5771 (gold)
5	dielectric	power/trace 1 dielectric layer	Fodel 6050 (dielectric)
6	via fill	power/trace 1 via fill layer	Fodel 5727 (gold)
7	conductor	ground and 2nd trace layer	Fodel 5771 (gold)
8	dielectric	ground/trace 2 dielectric layer	Fodel 6050 (dielectric)
9	via fill	ground/trace 2 via fill layer	Fodel 5727 (gold)
10a	conductor	bondable gold layer	Fodel 4596 (gold)
10b	conductor	solder pads layer	Fodel 4596 (gold)
11	dielectric	solder mask layer	Fodel 6050 (dielectric)

Table 3: List of hybrid layers. The bottom layer is layer 1, and the top layer is layer 11. Note that layers 10a and 10b are the same physical layer, but they are separated in the design for convenience.

Part	**Material**	X_0[1]	**Dimensions (l x w x t)**[1]	**Qty**	**% X_0**[2]	**% stave total**[3]	**% hyb total**
substrate	BeO	144	20 x 38 x 0.381	1	0.043	3.10	23.60
dielectric	glass	100	20 x 38 x 0.038	7	0.043	3.11	23.73
shield plane	Au[4]	3.35	20 x 38 x 0.008	1	0.018	1.31	10.01
power plane	Au[4]	3.35	20 x 38 x 0.008	1	0.018	1.31	10.01
ground plane	Au[4]	3.35	20 x 38 x 0.008	1	0.018	1.31	10.01
gold traces	Au[5]	3.35	20 x 38 x 0.006	2	0.005	0.39	3.00
SVX4 chips	silicon	93.6	9.11 x 6.4 x 0.3	4	0.019	1.15	8.77
conducting epoxy	silver[6]	8.54	9.11 x 6.4 x 0.025	4	0.002	0.11	0.80
ceramic caps 0402	dielectric	35	1 x 0.5 x 0.5	4	0.001	0.04	0.34
ceramic caps 0603	dielectric	35	1.6 x 0.8 x 0.8	9	0.006	0.41	3.09
ceramic caps 1206	dielectric	35	3.2 x 1.6 x 1.6	1	0.005	0.36	2.75
HV ceramic cap 1206	dielectric	35	3.2 x 1.6 x 1.25	1	0.004	0.28	2.15
resistors 0402	Al_2O_3	35	1 x 0.5 x 0.35	8	0.001	0.06	0.47
resistors 0603	Al_2O_3	35	1.6 x 0.8 x 0.45	6	0.002	0.15	1.16
resistor chip	silicon	93.6	2.29 x 1.52 x 0.254	1	0.0002	0.02	0.11
total					0.182	13.12	100

Table 4: A list of the contributions of the hybrid components to the radiation length of the stave.

[1]All dimensions are in mm.

[2]This is the percent of radiation length contributed to the total stave. This is calculated by the thickness divided by the radiation length, multiplied by the area of the component(s), multiplied by 6 (since there are six hybrids on a stave), divided by the total area of a stave.

[3]This is the the fraction that the component contributes to the total radiation length of the stave.

[4]This is multiplied by a factor of 0.47 to account for the volume fraction of gold in the paste.

[5]This is multiplied by the above factor of 0.47, plus an additional factor of 0.2 to account for the density of traces.

[6]This is multiplied by a factor of 0.1 to account for the fraction of silver in the epoxy.

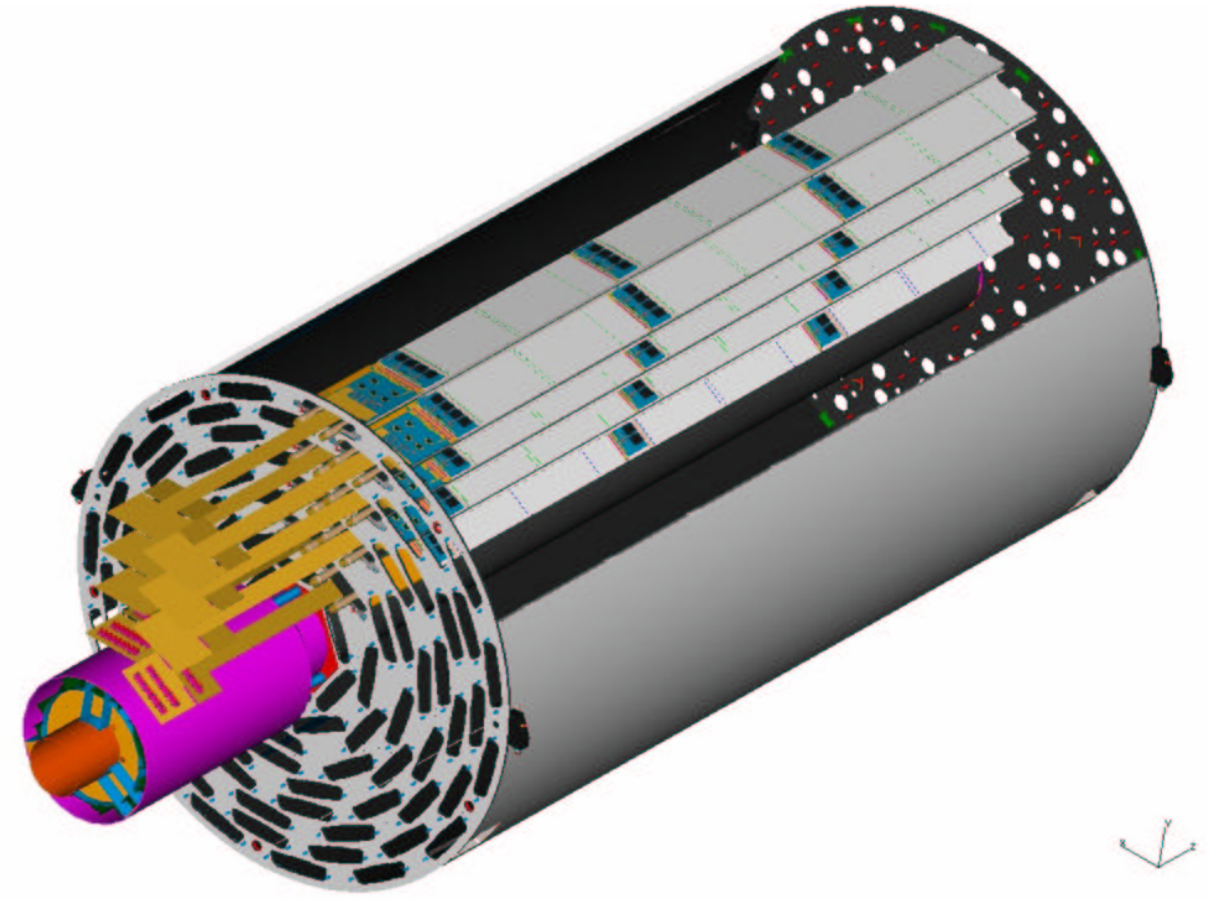

Figure 1: Exploded view of the CDF Run IIb silicon detector. Only five staves are shown. The mini-portcard is on the left in the picture; the first hybrid sits next to it, and the other hybrids are in the middle and to the right end of the stave.

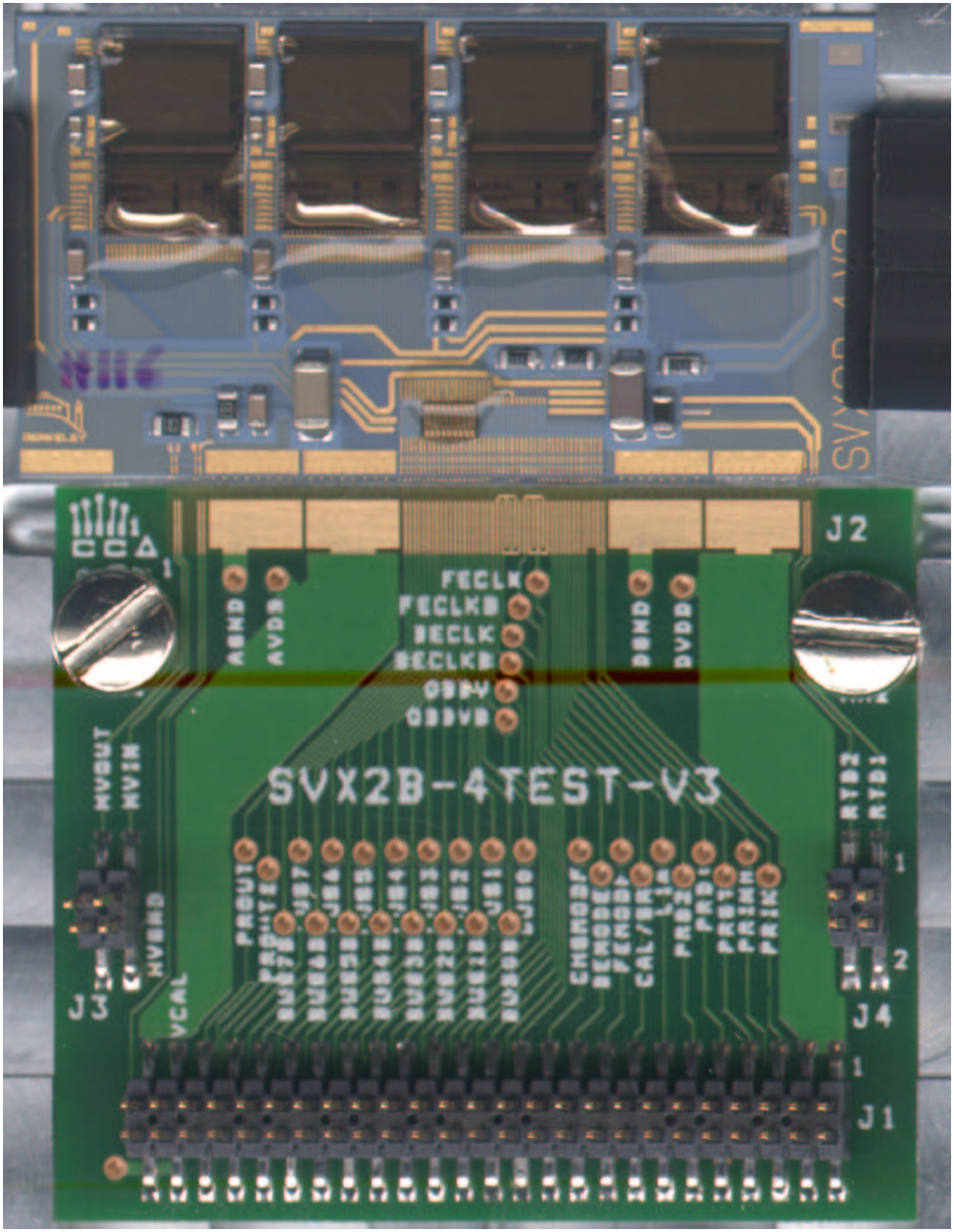

Figure 2: Photo of the four-chip hybrid (top) with testing printed circuit board (bottom).

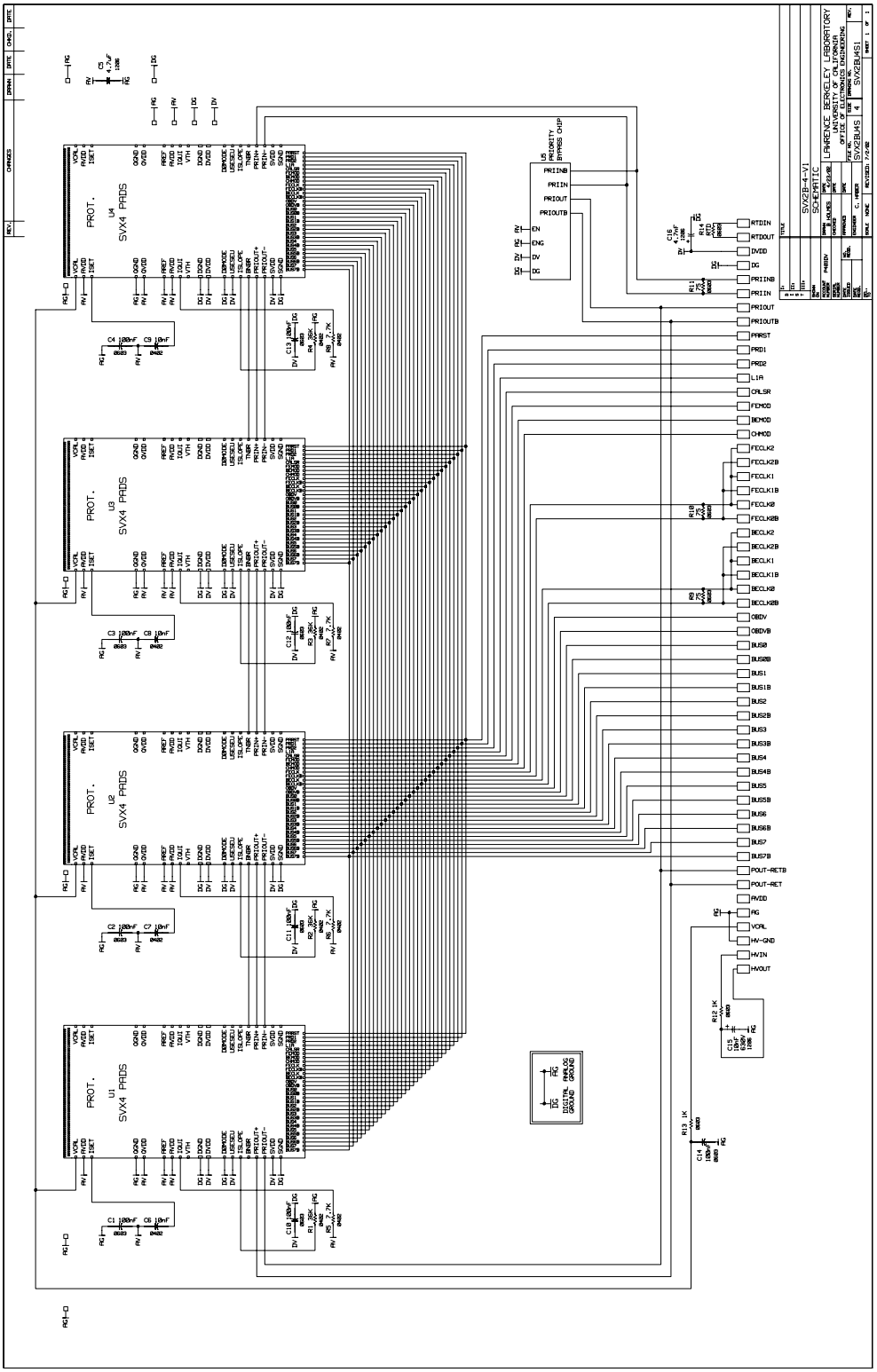

Figure 3: Schematic of four-chip hybrid. Note that the capacitor C5 shown here was eliminated due to space constraints. The termination resistor chip for the eight pairs of bus lines (bus0-bus0bar through bus7-bus7bar), which is only needed for the last hybrid on a stave, is not shown.

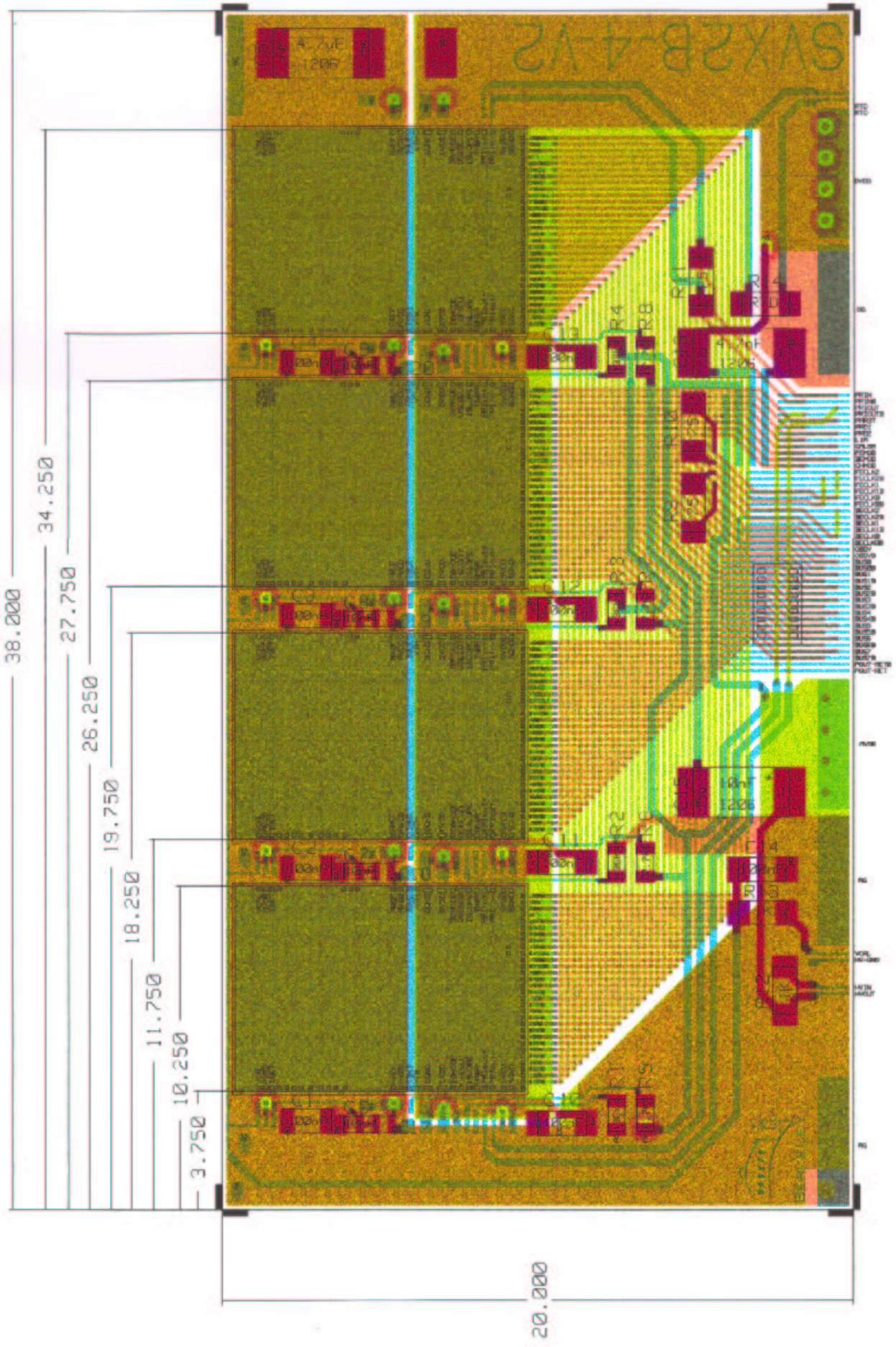

Figure 4: Layout overview (four-chip hybrid)

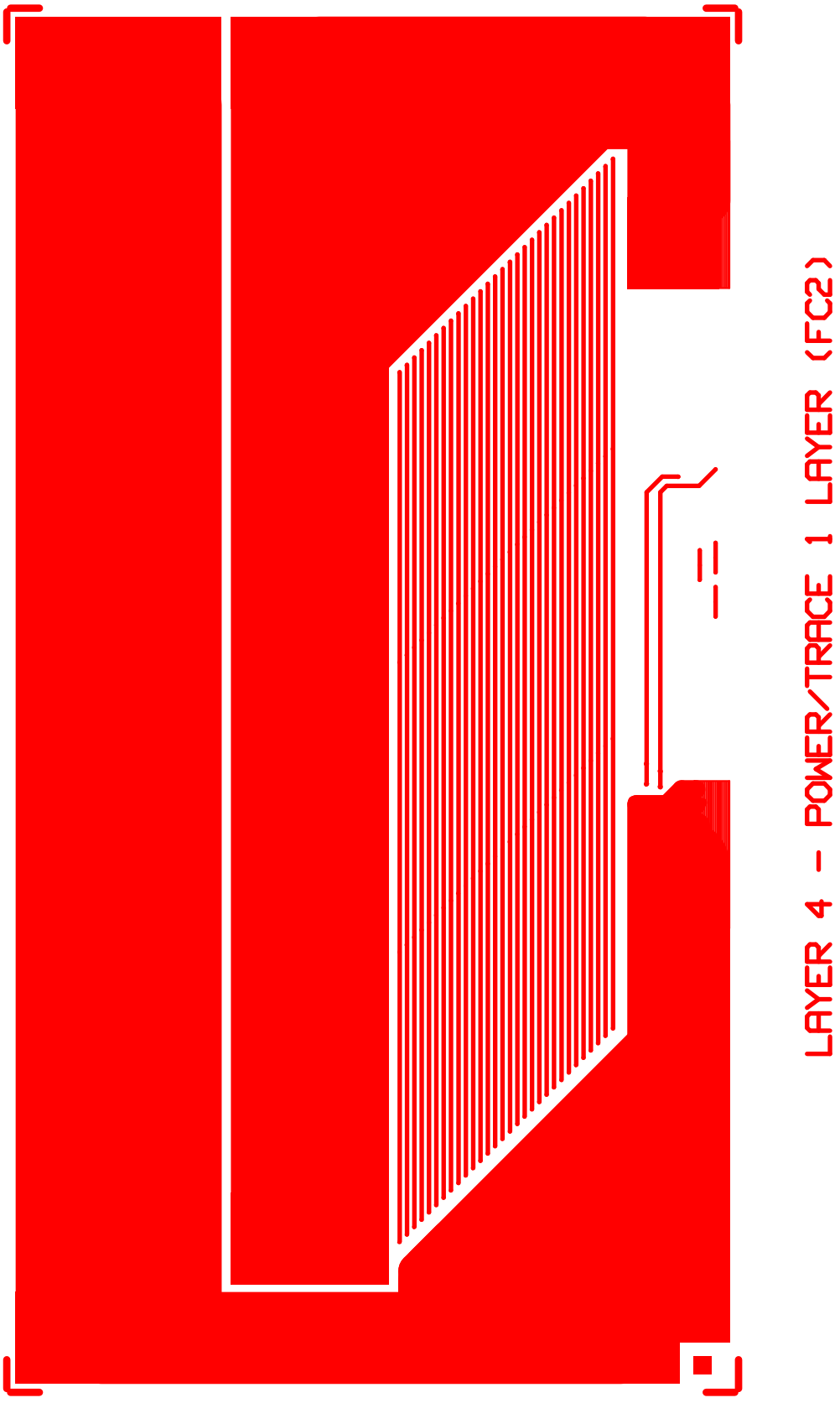

Figure 5: Power and trace layer (four-chip hybrid)

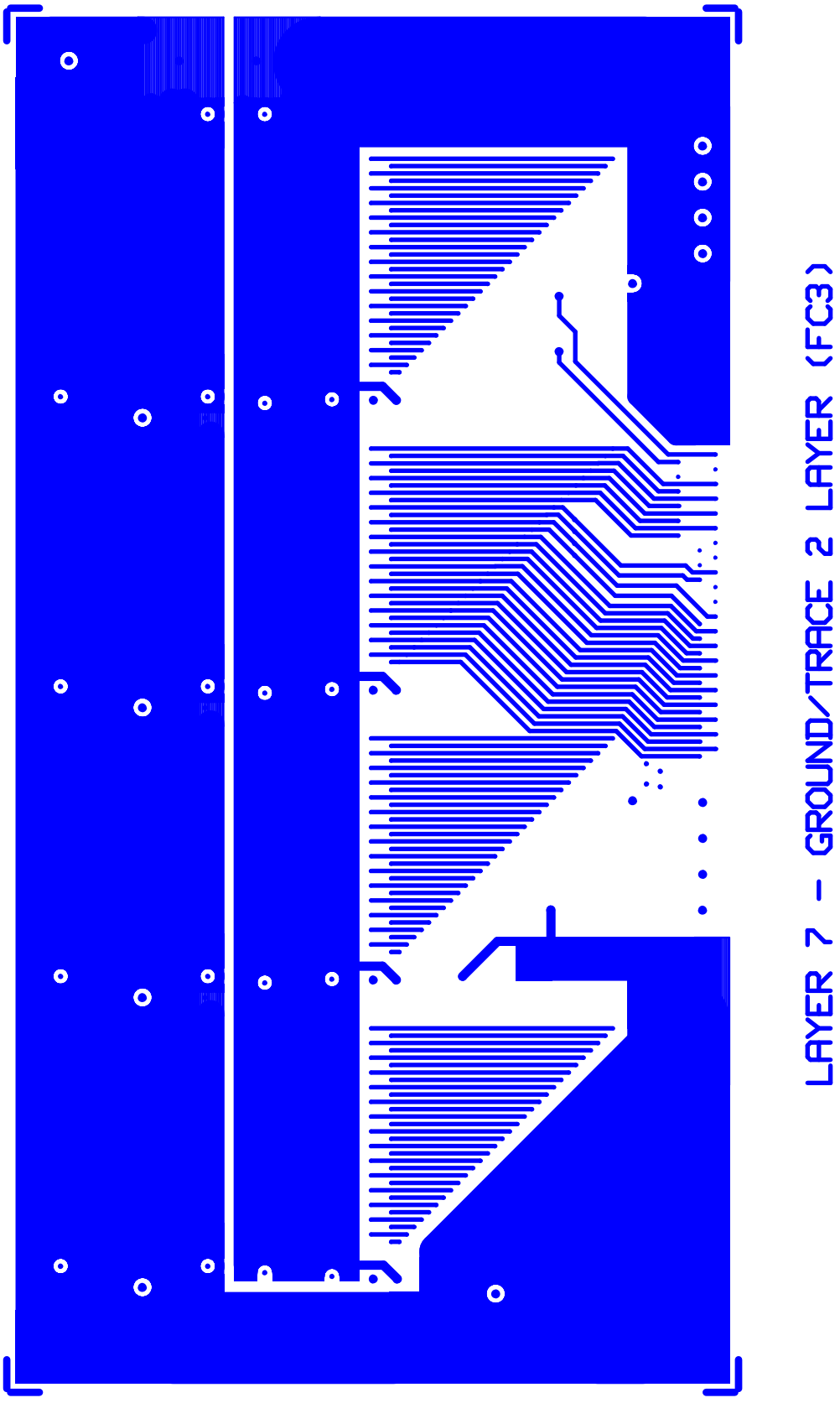

Figure 6: Ground and trace layer (four-chip hybrid)

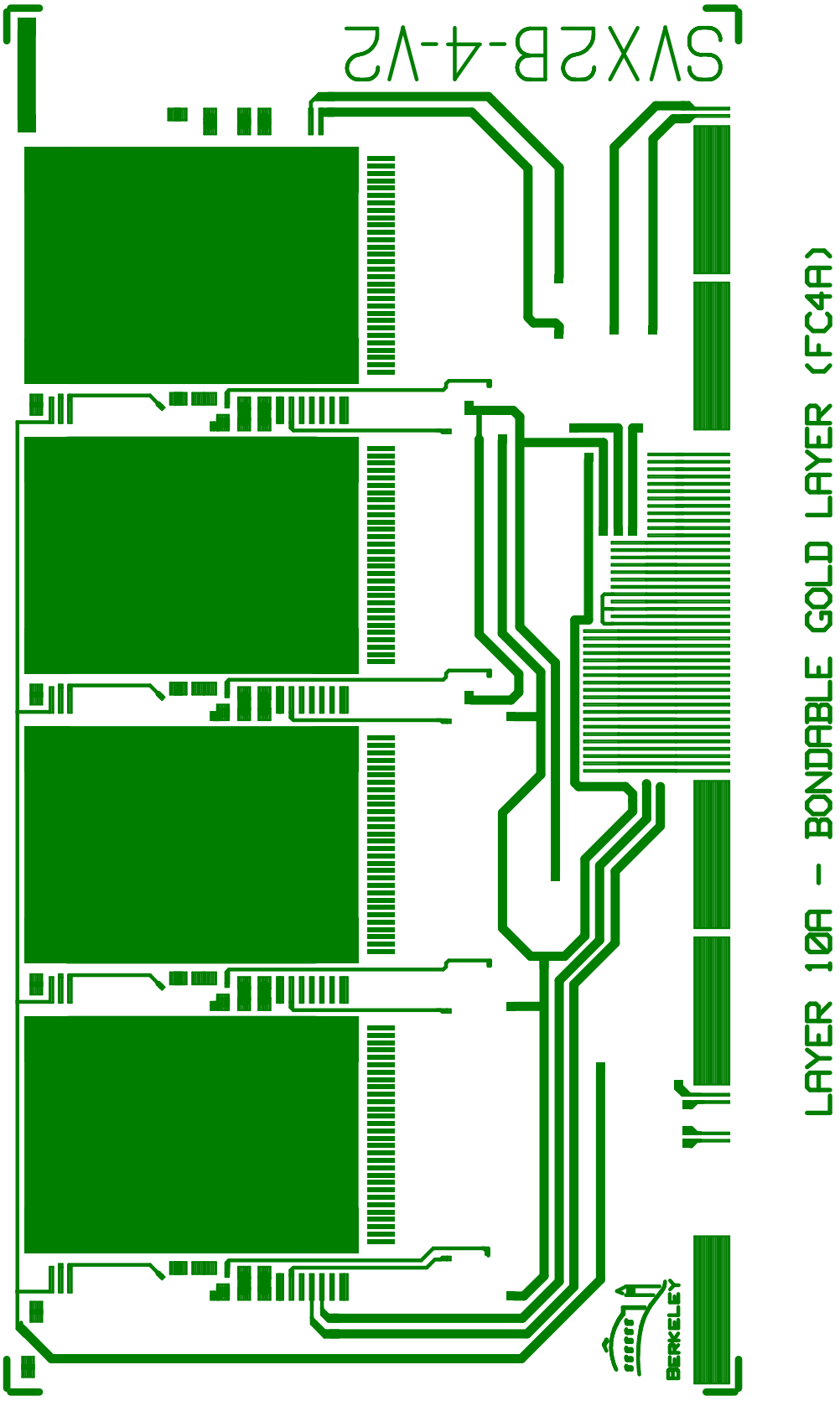

Figure 7: Bondable gold layer (four-chip hybrid)

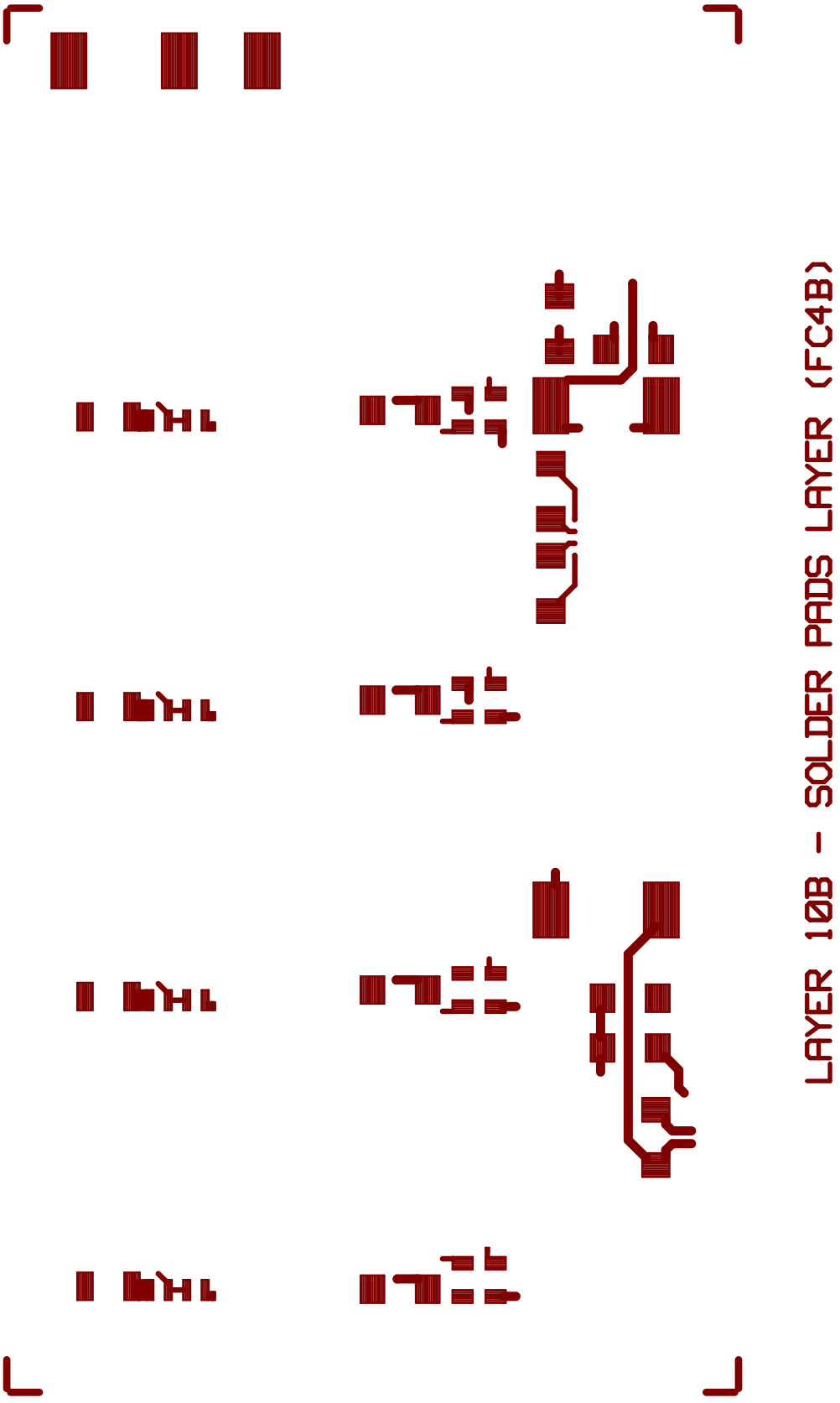

Figure 8: Solder pad layer (four-chip hybrid)

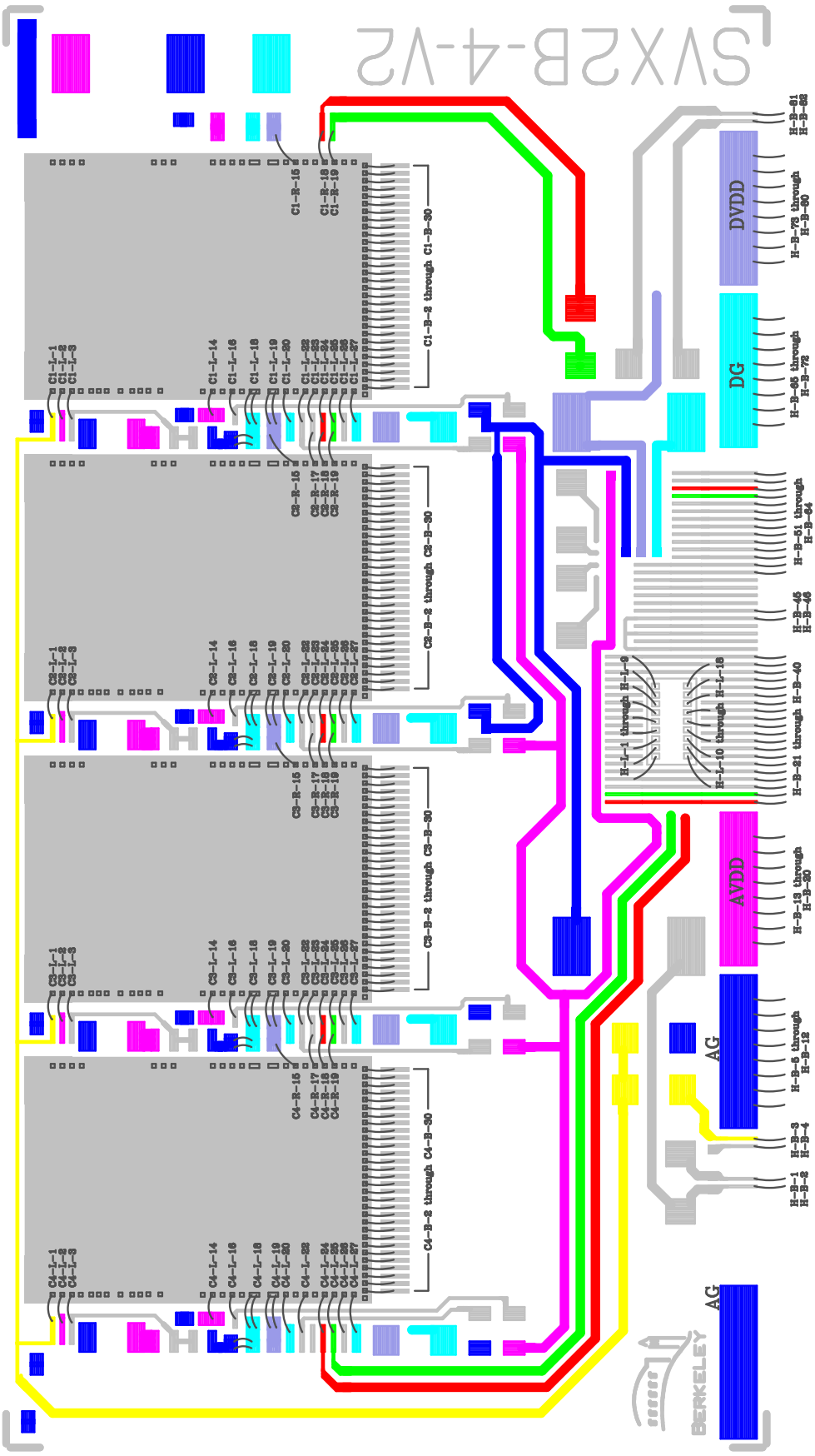

Figure 9: Bonding diagram (four-chip hybrid)

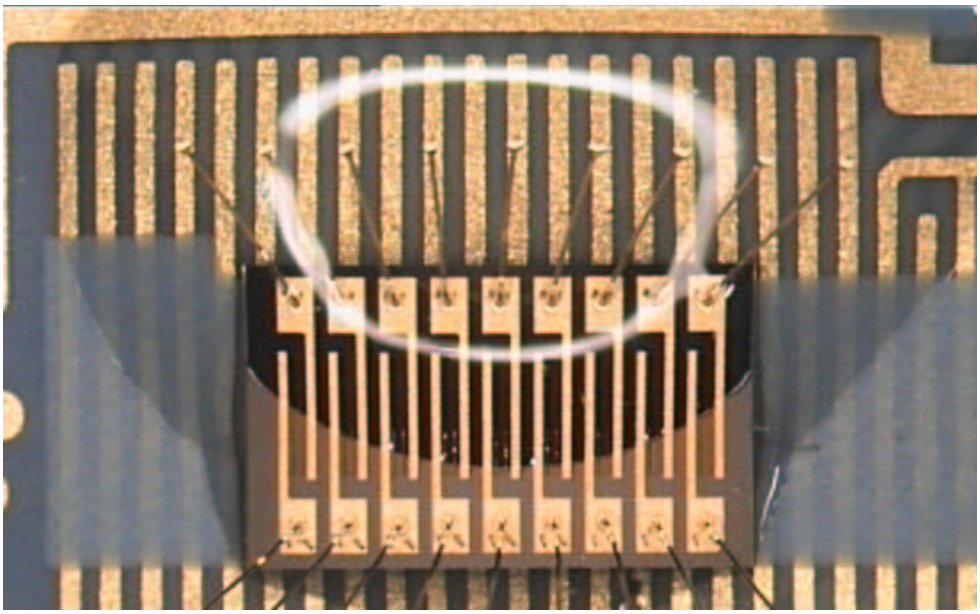

Figure 10: Encapsulation of the resistor chip array (four-chip hybrid). Note that only the upper row of bonds is encapsulated.

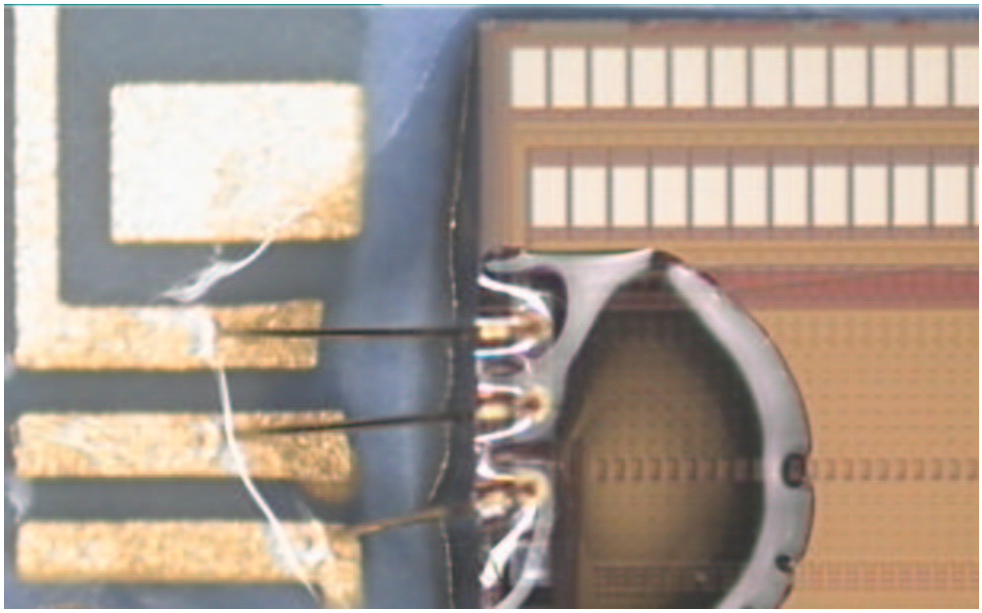

Figure 11: Encapsulation of the bond wires close to the SVX4 input pads (four-chip hybrid). Note how the encapsulant does not encroach on the input bond pads, making this a perfect encapsulation.

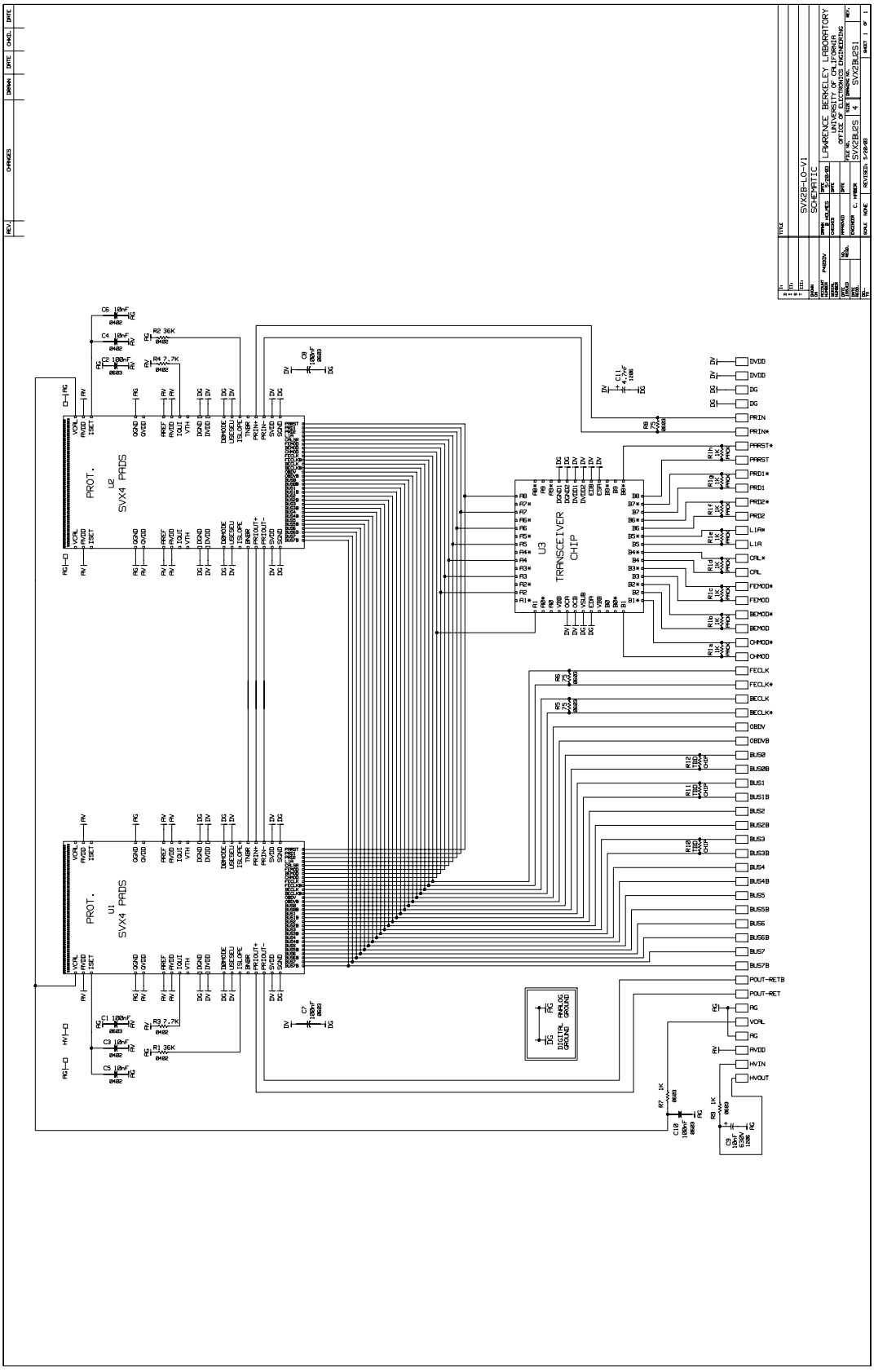

Figure 12: Schematic of L0 hybrid

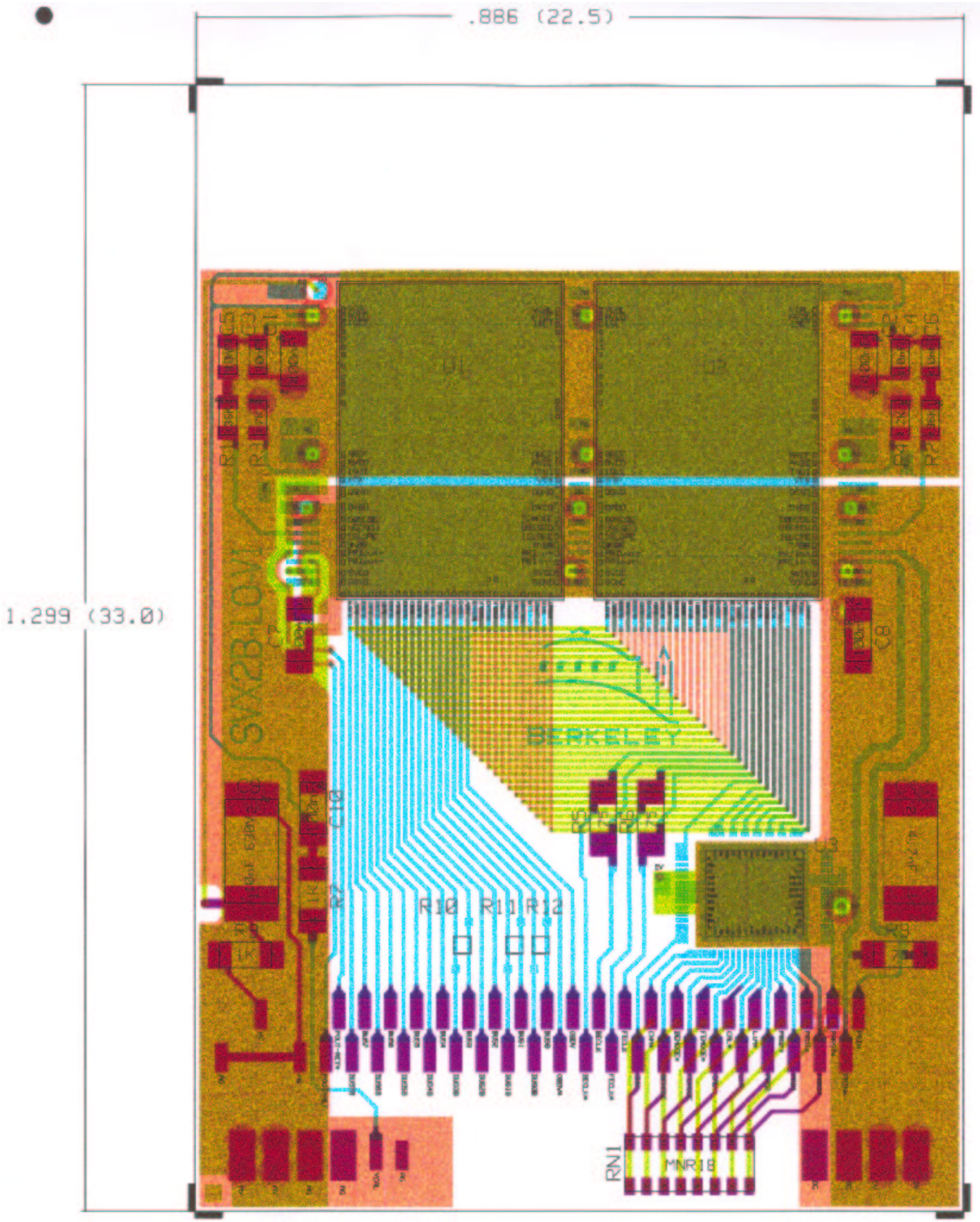

Figure 13: Layout overview (L0 hybrid)

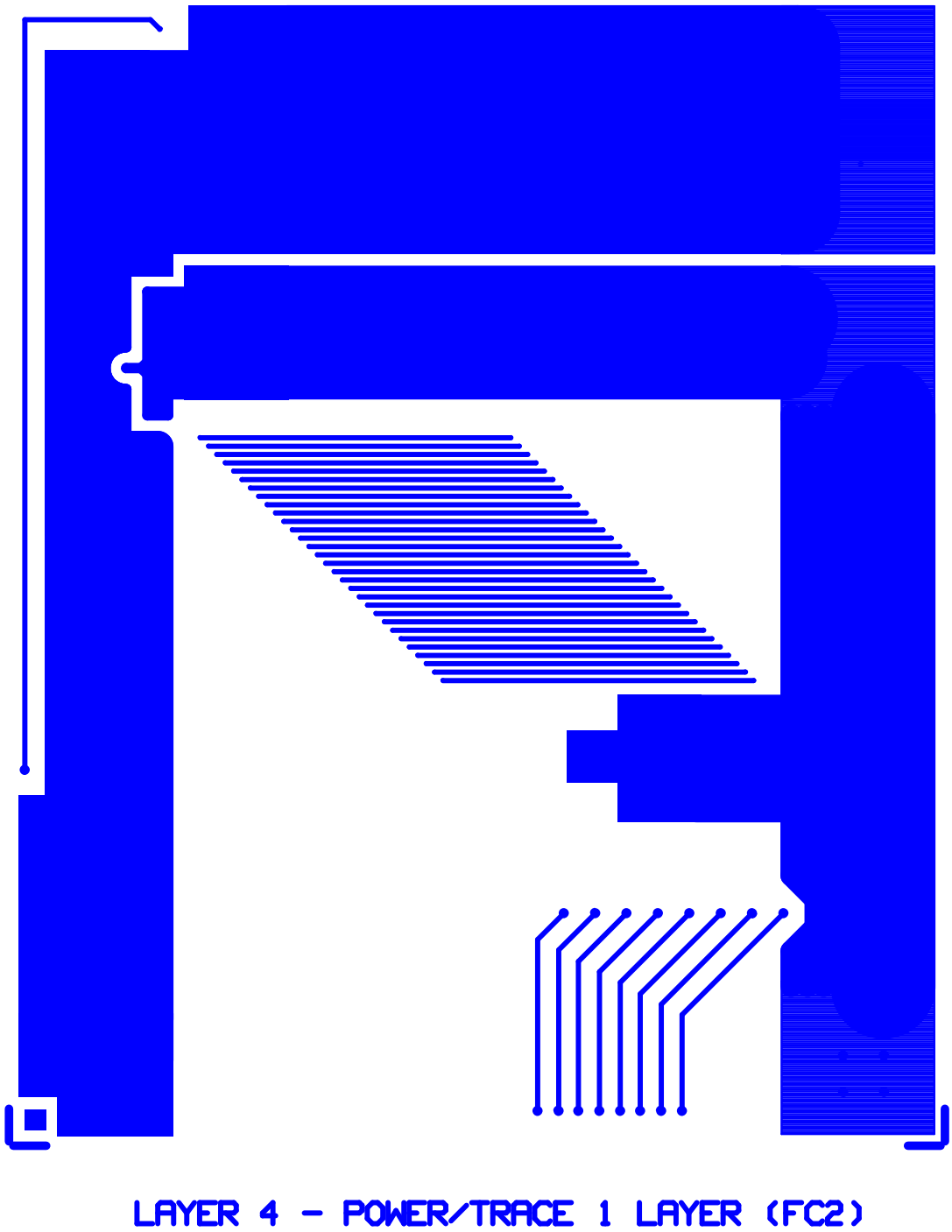

Figure 14: Power and trace layer (L0 hybrid)

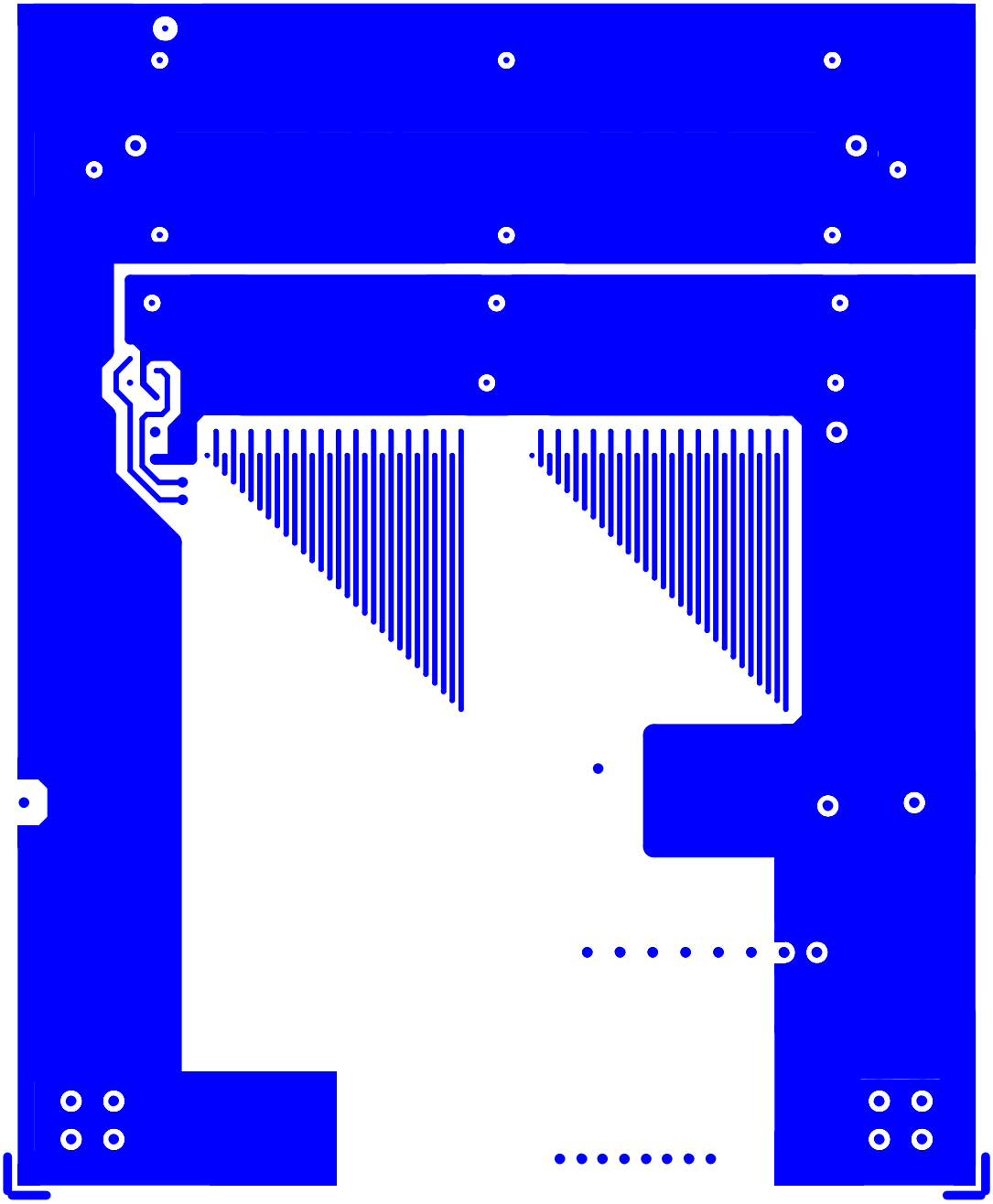

Figure 15: Ground and trace layer (L0 hybrid)

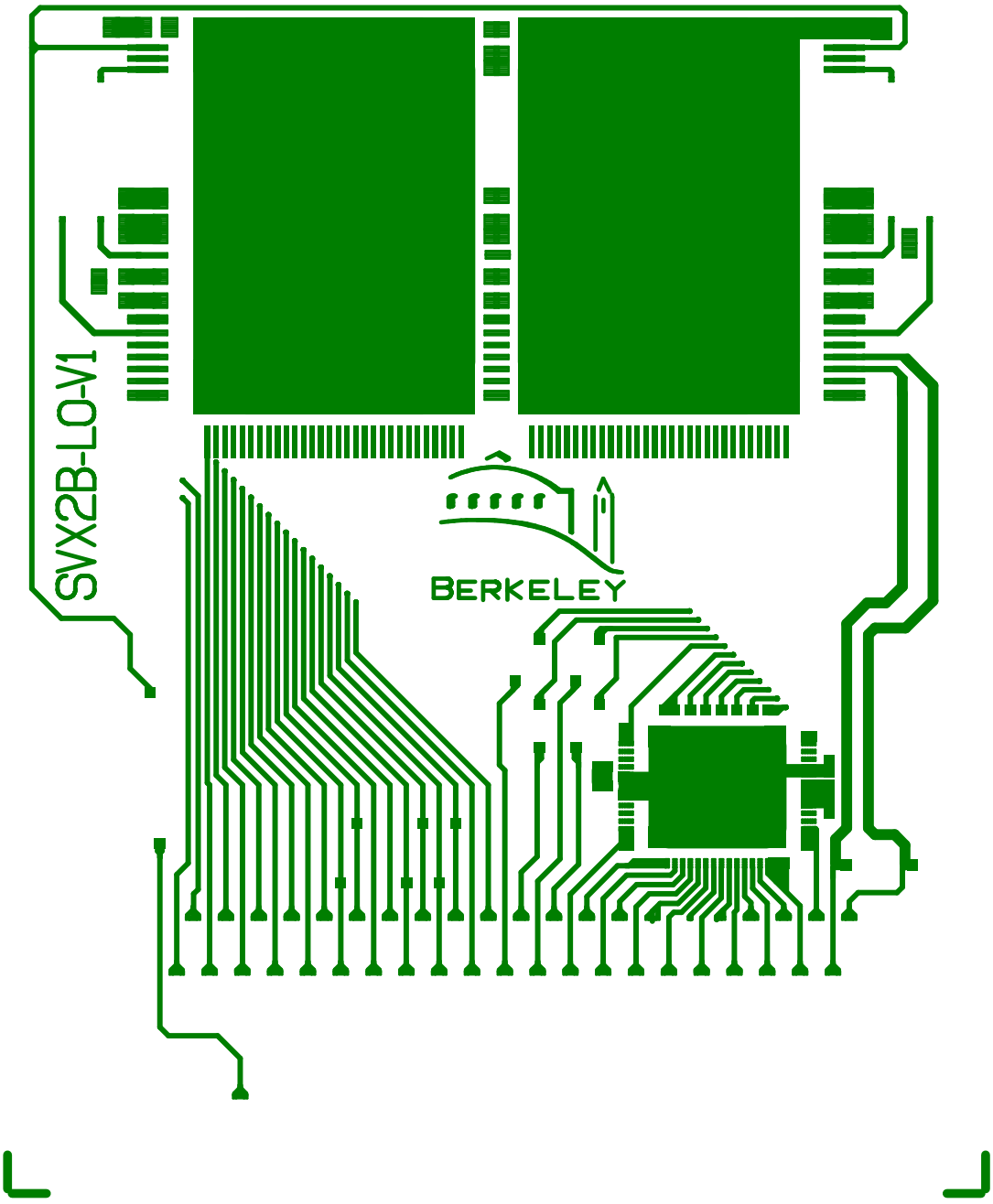

Figure 16: Bondable gold layer (L0 hybrid)

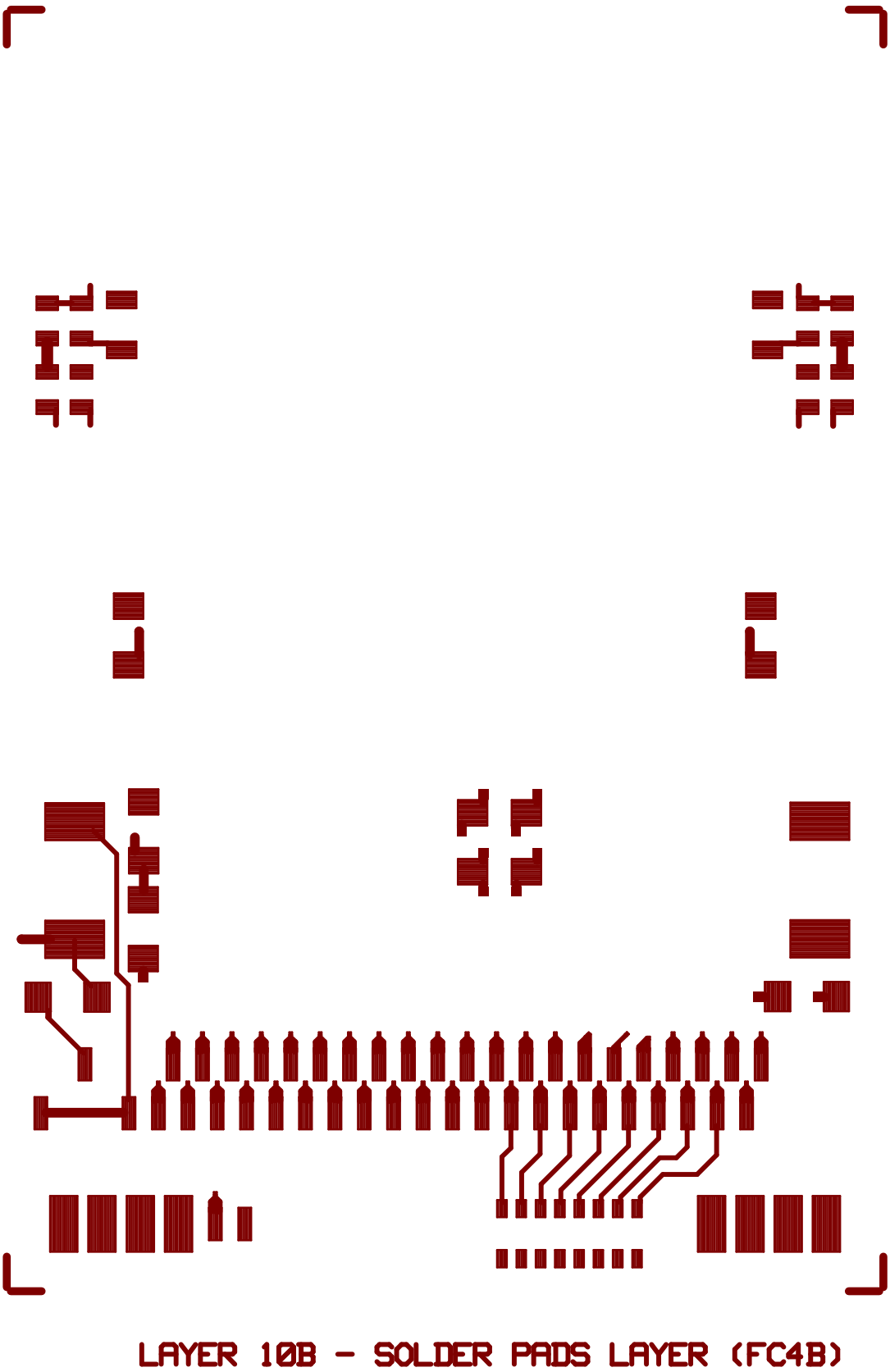

Figure 17: Solder pad layer (L0 hybrid)

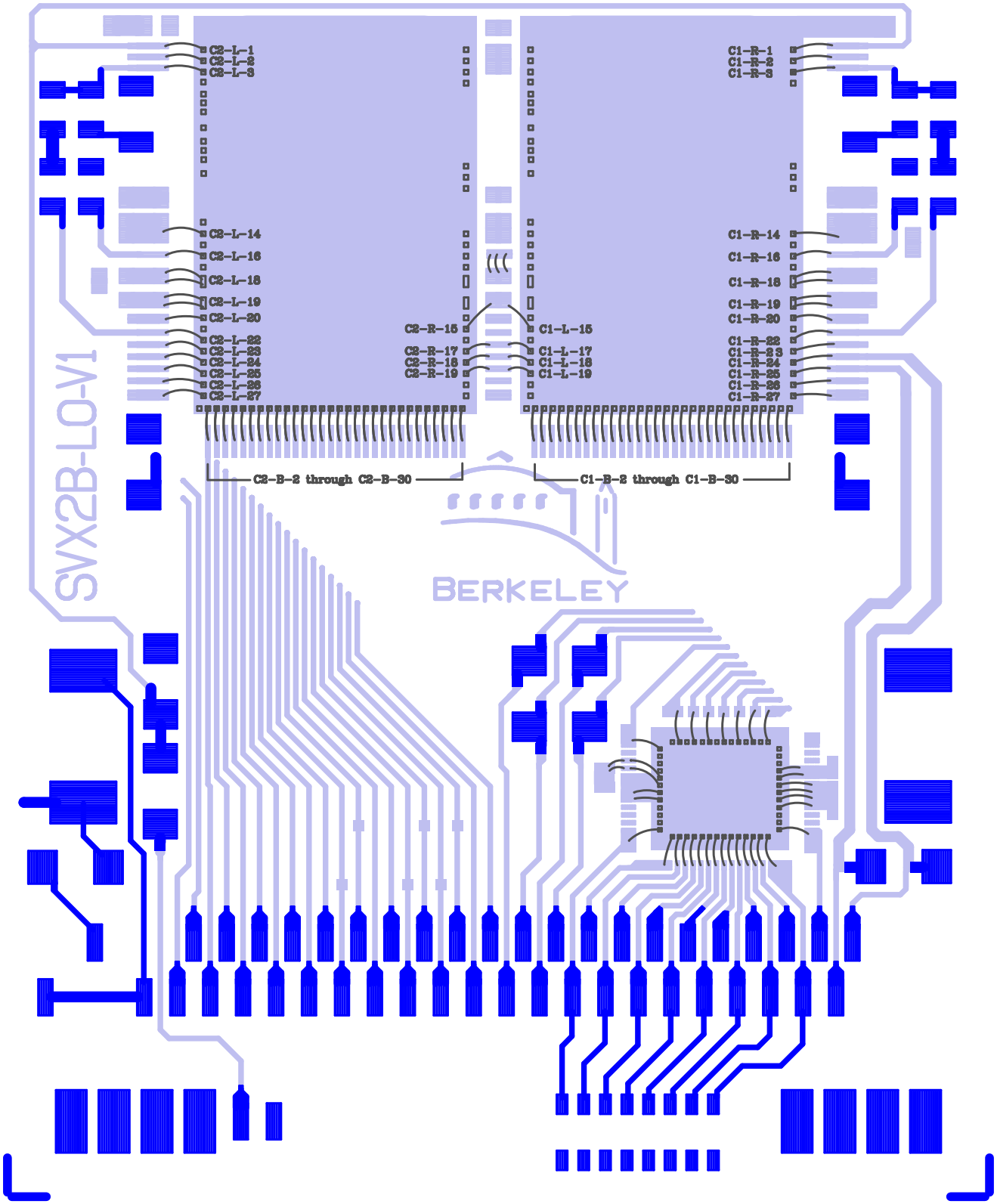

Figure 18: Bonding diagram of L0 hybrid. The upper alignment marks are omitted in this diagram.